WHAT IS CLAIMED IS:

1. A reference voltage generator which generates bias reference voltages in a semiconductor integrated circuit connected to first and fourth potentials to operate, comprising:

a first conductivity type first transistor whose source is connected to a second potential between the first and fourth potentials and whose gate and drain are connected to a first node;

a current-limiting resistor having one end connected to a third potential between the second and fourth potentials and the other end connected to the first node;

a first conductivity type second transistor having a source connected to the second potential, a gate connected to the first node and a drain connected to a second node from which a first reference voltage is outputted;

a second conductivity type third transistor having a drain and gate connected to the second node and a source connected to the fourth potential;

a second conductivity type fourth transistor having a source connected to the fourth potential, a gate connected to the second node and a drain connected to a third node from which a second reference voltage is outputted; and

a first conductivity type fifth transistor having a source connected to the first potential and a gate and drain connected to the third node.

2. A reference voltage generator according to claim 1, further comprising:

a sixth transistor which short-circuits between the second potential and the first node when a standby signal is supplied,

a seventh transistor which opens between the resistor and the third potential when the standby signal is supplied,

an eighth transistor which short-circuits between the first potential and the third node when the standby signal is supplied; and

a ninth transistor which short-circuits between the fourth potential and the second node when the standby signal is supplied.

3. A reference voltage generator according to claim 2, wherein the standby signal is a signal that changes between the second potential and the third potential, and further including a level shift circuit which is inputted with the signal and outputs a level-shifted standby signal changed between the first potential and the fourth potential and an inverted signal thereof.

4. A reference voltage generator according to claim 3, wherein the level-shifted standby signal and the inverted signal thereof are inputted to the gates of the eighth and ninth transistors.